

Slides 1-13:
Industry Buzz



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Slides 14-57
BER eSeminar

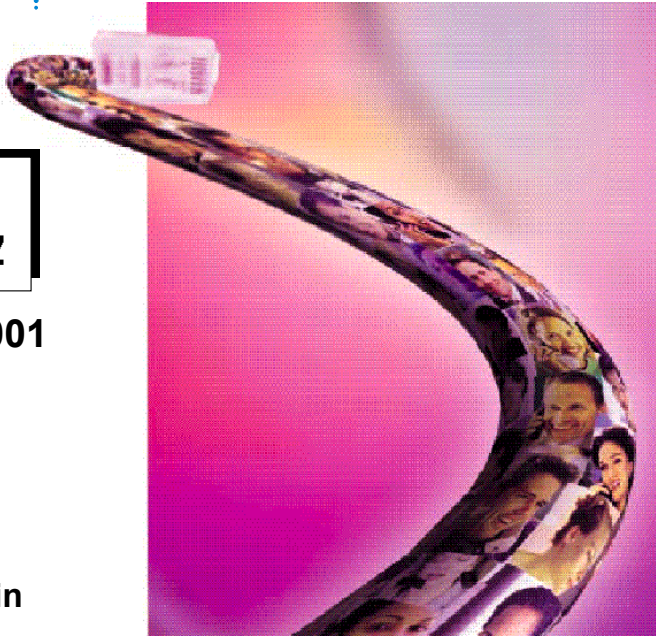
THE 40G
INDUSTRY BUZZ

November 6, 2001



presented by:

Larry DesJardin



THE 40G Industry Buss

- **Industry Update & Commentary**
- **“Late Breaking News” from Agilent**
- **Viewer Poll & Feedback**

THE 40G Industry Buss

- *Industry Update & Commentary* 
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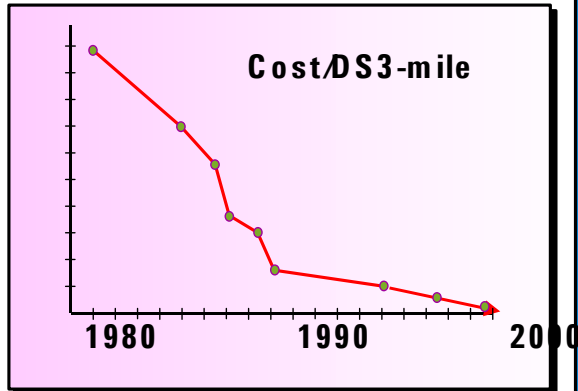
Why 40G?

Industry Update and Commentary

Why 40G?

Cost per Managed Bit!

- Each successive wave of higher speed has led to a lower cost/bit for transport equipment.



Industry Update and Commentary

Why 40G?

Cost per *Managed* Bit!

- **Fewer Wavelengths & Transponders**
 - Reduced Footprint & Rack Space
 - Reduced Power & Cooling
 - Reduced Fiber Interconnects
 - Reduced Inventory, Production and Repair
- **Increased Fiber Capacity**
 - Fewer Fibers, Amps -> Lower Cost

Industry Update and Commentary

Why 40G?

Summary

- **Mohr's law will drive the cost of 40G equipment to less than 4x that of 10G equipment.**
- **Additional costs of 40G will delay the cost/bit cross-over point in some applications.**
- **Other cost benefits will *help* 40G in some applications**
- **40G *will* happen. Only question is *when*, and in *which* applications.**

THE 40G Industry Buss

- Industry Update & Commentary
- *“Late Breaking News” from Agilent*
- Viewer Poll & Feedback



Late Breaking Agilent News

2 New DCA Modules

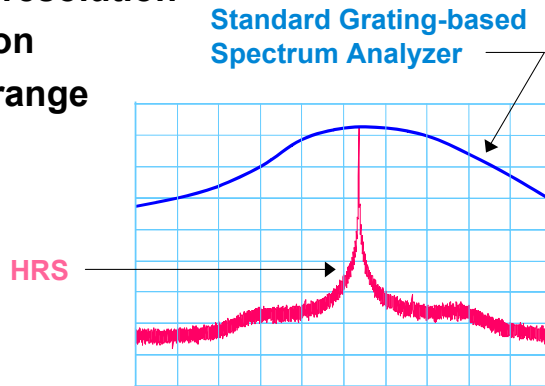
- **Agilent 86116A Input Module**
 - 55 GHz Optical BW
 - 65 GHz Electrical BW
- **Agilent 86107A Precision Timebase Reference Module**
 - Jitter reduced to 200fs RMS
 - Timebase Resolution to 2ps/div.



www.agilent.com/cm/rdmfg/industry/40gbs.shtml

Late Breaking Agilent News

- **Agilent 83453A High Resolution Spectrometer**
 - Sub-picometer resolution
 - 10Mhz resolution
 - 60db dynamic range



www.agilent.com/cm/rdmfg/hrs

THE 40G Industry Buss

- Industry Update & Commentary
- “Late Breaking News” from Agilent
- *Viewer Poll & Feedback*



Viewer Poll and Feedback

What year

a) will the first 40G Equipment be deployed?

and

b) when will 40G become mainstream?

- **Send responses to
larry_desjardin@agilent.com**
- **Individual responses remain confidential, only
summary of results displayed.**
- **Results to be shown next month!**

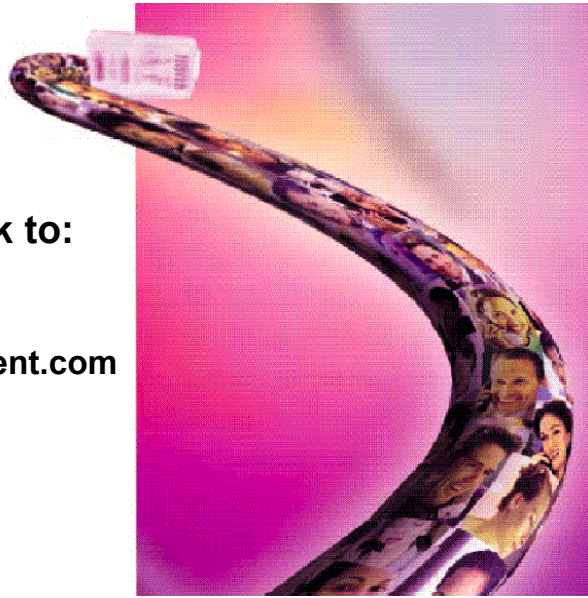


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THE 40G **INDUSTRY BUZZ**

Send any feedback to:

larry_desjardin@agilent.com





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**Effective Ways of Testing
BER on 40Gb/s High-
Speed Interface Devices**

November 6, 2001

presented by:

**Lee Nichols
Boyd Troop**

Outline

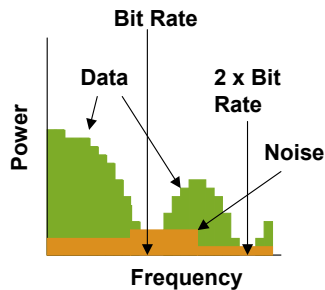
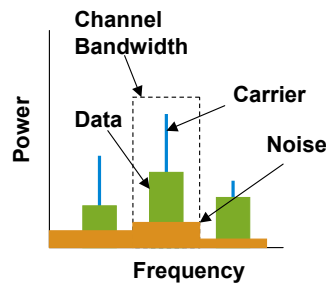
- **Introduction**
- **Measurement Approaches for Digital Communications**
- **Simulating Real Data Streams**
- **Measuring Bit Errors**
- **40 Gb/s Waveforms and Technology**
- **Flexible BERT Design**
- **Device Testing Architectures**
- **Conclusion**

Introduction

- **Testing at 40Gb/s presents tough challenges**
- **Device testing is critical for predicting overall system performance and reliability**
- **Existing technology can be used to test 40Gb/s devices**

Spectral Vs. Time-Based Measurements

- Spectral measurements
 - Channelized systems
 - Signal-to-noise
 - Narrowband
 - Performance insight
 - Product development



- Time-based measurements
 - Baseband systems
 - Eye opening, bit error
 - Wideband
 - Performance verification
 - Product delivery

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In a carrier multiplexed system, signal quality is typically assessed channel-by-channel using spectral measurements of signal power versus noise power because such systems are inherently narrowband. Spectral measurements can offer detailed performance insights and align well with R&D testing objectives.

In a high-rate baseband system where the spectral content of a single high-capacity channel is inherently wideband, time-based measurements account for variations across the entire spectrum with a single measurement. Time-based measurements offer more direct comparison to operational performance and align well with manufacturing test philosophies.

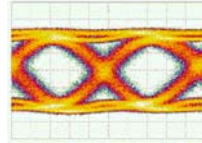
In general, the relative advantage of these measurement approaches depends upon the user's test objectives in terms of cost, time, and/or complexity of data output.

Also note that many systems (WDM and broadband, for instance) can be considered both channelized and baseband and can therefore take advantage of multiple measurement approaches.

Common Digital Measurements



- Bit Error Ratio (BER)
- Eye Diagram Analysis
- Jitter



Among communications device and system manufacturers, time-based or time-domain measurements of digital waveforms have become standard.

These measurements can be thought of as outward manifestations of underlying spectral characteristics.

The most common are:

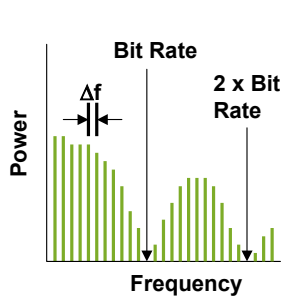
Bit Error Ratio - a black box approach to quality measurement via bit-by-bit comparison

Eye diagrams - a method of investigating pulse transmission amplitude characteristics

Timing jitter - a time-domain alternative to phase noise measurement for investigating pulse transmission timing characteristics

Simulating Real Data (PRBS)

- Pseudo-random binary sequence (PRBS)
 - Pattern length $2^N - 1$
 - Every possible sequence of N bits
 - Wide spectral content



- Key spectral features:

- $\Delta f = \text{bit rate} / \text{pattern length}$
- Nulls at bit rate harmonics
- Envelope is pulse shape transform

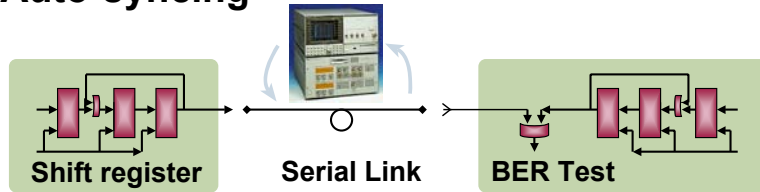
Because high-rate baseband systems are inherently wideband, it is important to fully exercise the system componentry by simulating the wide spectral content of real communication streams.

Communications test equipment typically generates pseudo-random bit sequences containing every possible sequence of N bits for this purpose.

Key spectral features of the PRBS are determined by the bit rate, the pattern length, and the basic pulse shape.

Simulating Real Data (Enhancements)

- Hardware shift registers
- Auto-syncing



- User-definable mark densities
- Long mark sequences
- Integrated protocol generation/analysis
- User-programmable pattern memory

Bit Error Rate Testers (BERTs) use hardware shift registers to generate PRBS streams and to provide an auto-syncing analysis path for the returned data.

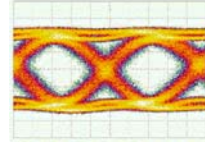
For stressing clock recovery circuits, BERTs offer patterns with user-definable mark densities or long mark sequences.

To test network elements with desired control responses to frame or packet overhead, BERTs may offer integrated protocol generation/analysis.

BERTs may also offer memory access for completely user-defined patterns

What Is a Bit Error Rate?

- **Bit Error Rate (BER)**
 - Black-box transmission quality metric
 - Electrical and optical transmitters/receivers
 - Network elements and transport media
- **Sources of bit errors**
 - Linecard hardware faults
 - Jitter, wander, amplitude noise
 - Signal degradation in transmission
- **Error detection and correction**
 - Frame or packet retransmission
 - Piggyback coding

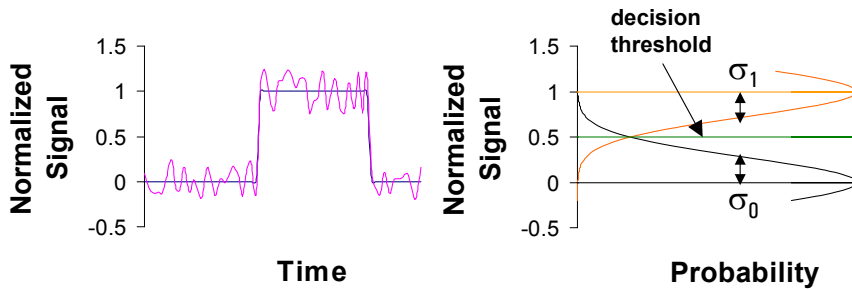


In general terms, bit error rate is a black box measurement of transmission quality used to verify the performance of key elements of a transport link. BER measurements can be used to verify both electrical and optical transmitter or receiver hardware as well as to quantify the influence of intermediate elements such as amplifiers, switching fabrics, or even the transmission lines themselves.

Bit errors can be caused by hardware faults in network element line cards; jitter, wander and other types of noise which may or may not be pattern dependent; or signal degradation due to transmission effects such as attenuation, dispersion, or crosstalk.

Errors can be corrected on-the-fly and transparent to the user via software or hardware detection/correction algorithms that may rely on retransmission of data or piggyback coding (FEC or ATM HEC, for instance) for data regeneration.

When Good Bits Go Bad



- Bit marks (0 or 1) determined by
 - decision threshold
 - signal level at sampling instant
- Statistical distribution determines error probability
- Statistics of signal + noise vary with
 - Sampling instant within unit interval (UI)
 - Mean amplitude

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Bit marks (zero or one) are determined by the analyzer's decision threshold and the signal level at the sampling instant

As signal-to-noise ratio (SNR) decreases, the sampled signal will more frequently fall out of its intended mark range resulting in an error.

The probability of such errors can be calculated based on the statistics associated with the accumulated noise.

These statistics may vary with the average amplitude at the sampling instant and where that sampling instant falls within the bit period or unit interval due to the dependence of noise in some components (shot noise in APDs, for instance) upon signal level and the presence of jitter.

BER and Sensitivity

$$\text{BER} = \frac{\text{number of bits received in error}}{\text{number of bits received}}$$

- **Statistically valid measurements**
 - $T_{\text{MIN}} = N / (\text{bit rate} \times \text{BER}_{\text{MAX}})$
 - Low bit rates require extrapolated performance
- **Sensitivity**
 - Minimum average signal level for maximum BER
 - Degrades with higher data rate systems

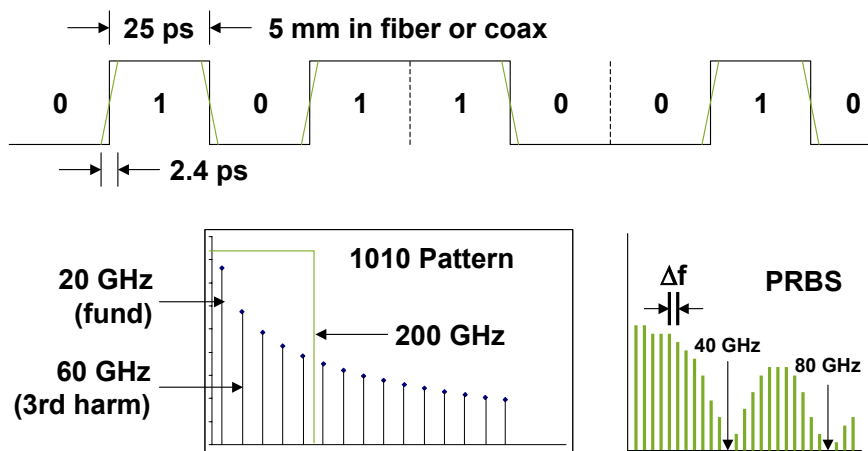
The bit error rate is the experimental measure of the error probability based on the accumulated errors within a statistically valid sample of bits. Commonly, a statistically valid sample is taken to be the number of bits accumulated to obtain 100 errors. In general, one can calculate the minimum test time required to verify a maximum BER based on the bit rate and a statistically valid number of errors N.

For lower bit rates, the single-shot test time (for instance, to verify less than 1e-9 BER at 155 Mb/s using 100 errors requires over 10 minutes) may be unacceptable. In these situations, performance is typically extrapolated from measurements taken under artificially degraded signal-to-noise conditions.

System sensitivity is typically defined as the minimum average signal level (average of 1 and 0) at which a maximum BER is achieved. This would be the average electrical amplitude or the average optical power depending upon where in the system the sensitivity is being measured.

Sensitivity typically degrades somewhat with higher data rate designs simply due to the intrinsically wider noise bandwidth.

NRZ Data Streams at 40 Gb/s



- Requires resilient clock recovery design
- Bandwidth determines transition time

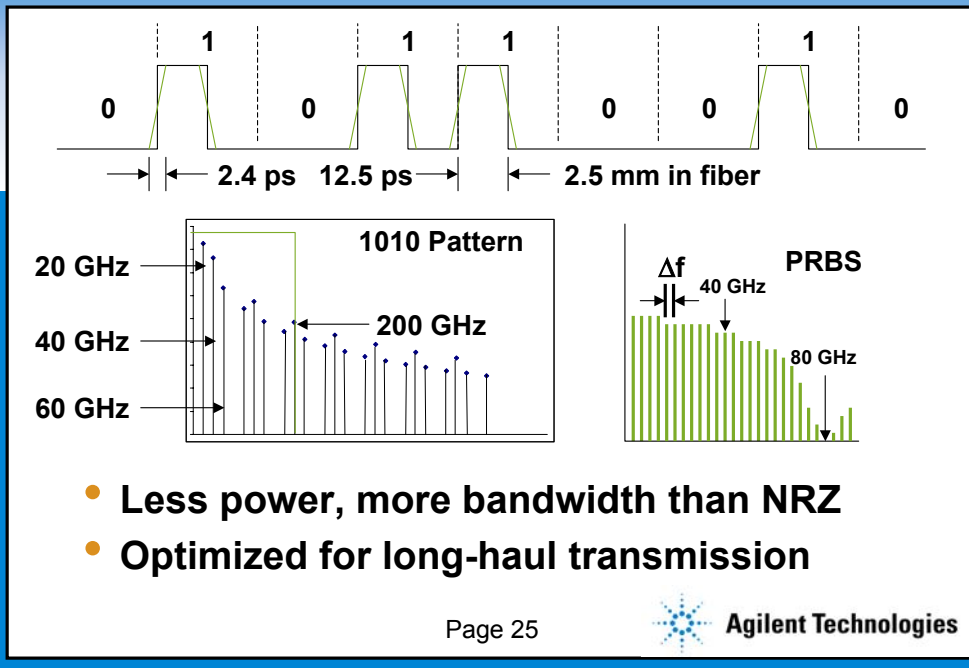
In a non-return-to-zero data stream, either mark is generated by maintaining the associated signal amplitude during the entire unit interval excepting the unavoidable rise and fall times when the mark changes. In this data format, the average signal level is simply half the sum of the levels associated with the marks. As it is possible to get strings of ones or zeroes without intervening transitions (for example, where the dashed UI boundaries are shown above), clock recovery circuits must be designed with this in mind.

Given the speed of electromagnetic waves in optical fiber or coaxial cable, the 25 ps UI associated with a 40 Gb/s stream extends over roughly 5 mm. Over a typical optical transmission distance of a few km, even thermal material changes may be significant contributors to signal jitter or wander as percentage of UI.

In the frequency domain, an ideal 1010 pattern appears as an infinite comb of odd harmonics of the fundamental frequency which is one-half of the bit rate. Thus, the spectrum of a 40 Gb/s 1010 pattern contains components at 20, 60, 100 GHz and so on. When the data is pseudo-randomized, each component becomes a lobe containing multiples of the pattern repetition frequency.

Real systems operate with bandwidth limitations which generate longer transition times between bits as a result of the loss of high-frequency spectral components. With a 40 Gb/s data stream, even a relatively heroic bandwidth of 200 GHz results in 0.1 UI of transition time.

RZ Data Streams at 40 Gb/s



Return-to-zero format relies on intra-symbol transitions during mark ones to improve clock recovery. One drawback to this format is the minimum system bandwidth required: while a designer can get away with a single spectral lobe and still reproduce some semblance of a pulse (albeit with significant transition times), that lobe is twice as wide in an RZ scheme simply due to the shorter pulse widths.

Nevertheless, RZ formatting has significant advantages for long-haul transmission including:

lower average transmitter power than NRZ for the same mark one amplitude (specifically, half the optical power or a fourth of the electrical power);

lower power experiences higher gain in optical amplifiers which are typically operated in saturation;

short pulses minimize degradation due to chromatic dispersion;

short pulses lend themselves to optical soliton transmission techniques.

Electronics at 40 Gb/s

	Si	SiGe	GaAs	InP
History	Many Years, Many foundries	A few years, 3 foundries	Many years, Many foundries	On the edge, some research labs
Technology ft today(3ys)	20(50)GHz	100(250)GHz	100(600)GHz	150(600)GHz
Complexity	high	Low to medium	low	low
Reliability	proven	proven	proven	'in doubt'
Commercial	low		x10	
Electron Mobility (cm ² /V-s) @RT	1350	2000-3000	8500	4000

- **Compound semiconductor devices benefit from higher electron mobilities**



Amplifiers at 40 Gb/s

- **Microwave/mm-wave amplifiers**
 - Sub-100 kHz low-frequency cutoffs
 - +20 dBm (100 mW) power output
- **Capacitive coupling**
 - Protect transistor from DC currents
 - Isolate amplifier stages from external impedances
 - Prevent DC saturation of available gain
- **Limited design flexibility**



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The types of wideband amplifiers used for high data-rate applications are equivalent in design to those that have been used for years in aerospace/defense applications. Unlike standard low-noise RF amplifiers, those used for high-speed digital communications require very low low-frequency cutoffs in order to support random data streams and higher saturated output powers to drive optical modulators.

Higher-speed (microwave/mm-wave) amplifier technologies require DC blocking or AC coupling capacitors at their inputs and outputs.

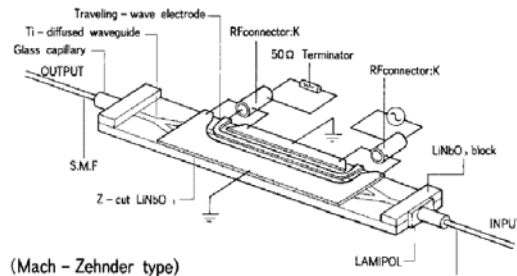
These components serve to protect the sensitive transistor technologies employed in these types of amplifiers from substantial DC or low-frequency transient currents;

isolate the amplifier stages from external impedances, thereby holding performance over a variety of excitation/load conditions; and protect the available signal gain from DC saturation.

Unfortunately, AC coupling limits available locations in the system architecture for implementing adjustable decision thresholds which are required for detailed signal quality measurements

Optical Transmission at 40 Gb/s

- **Distributed feedback lasers inappropriate**
 - Current modulation generates chirp
 - Laser relaxation time limits modulation bandwidth
- **High-speed external Mach-Zehnder modulators**
 - Utilize electro-optic effect
 - Specialized waveguide/electrode designs



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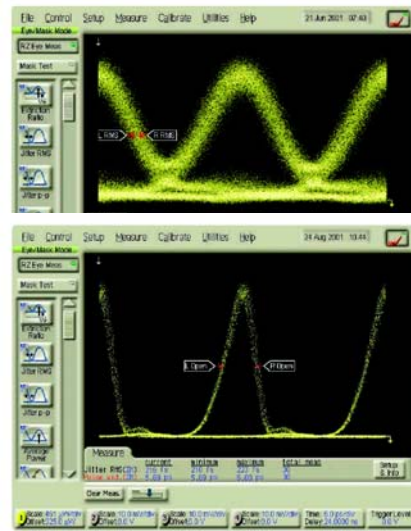
CATV and telco vendors have relied on very high-speed direct (current) modulation of distributed feedback (DFB) lasers for lower data rate systems, but this technique is limited by the inherent frequency chirp associated with current injection of semiconductor lasers and the internal dynamics of the lasing medium to around 10 GHz.

The modulation bandwidth demands of 25 ps pulses requires the use of external modulators such as LiNbO₃ Mach-Zehnder modulators (MZMs) employing the electro-optic effect which have potential bandwidths in the 100s of GHz.

The highest-speed modulators rely on velocity-matched traveling-wave designs where the coupling between the microwave and optical fields is maximized by using waveguide geometries such that the two waves travel through the device at nearly the same speed.

Optical Detection at 40 Gb/s

- Sequential or random repetitive sampling architectures
- Digital communications analyzers
- High electron-mobility InGaAs photodetectors



40Gb/s RZ signal using an optical sampling architecture.

Given the raw speed of real-time sampling A/Ds, capturing data streams at OC-48 and above necessitates the kind of sequential or random repetitive sampling architectures used in high-speed digital communications analyzers (DCAs).

However, at OC-768, even these types of measuring instruments may be somewhat limited when it comes to measuring the very highest speed waveforms, such as RZ patterns due to insufficient detection bandwidth. Minimum transition times and internal timebase jitter must be considered when evaluating DCA measurements.

Higher-speed optical sampling techniques have been developed using nonlinear optical materials at various laboratories.

As with electronics parts, high-speed photodetector designs rely on high electron mobility compound semiconductors and designs.

Jitter Measurement at 40 Gb/s

- DCA with enhanced timebase provides limited jitter measurement
- Phase noise measurement system
 - Detailed signal timing analysis
 - Accurate jitter measurement



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While the inherent timebase jitter in a high-speed DCA may be sufficiently small for waveform analysis, it will not generally allow for accurate measurement of the random jitter associated with the signal. This can be improved using available timebase enhancement modules.

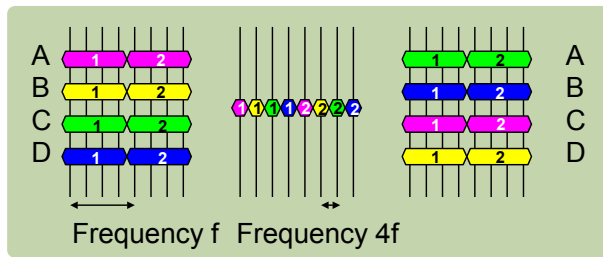
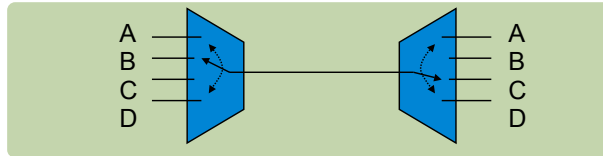
For in-depth analysis of jitter issues, it may be necessary to use a phase noise measurement system which can isolate the timing component of system noise from the amplitude component.

Real World Device Testing

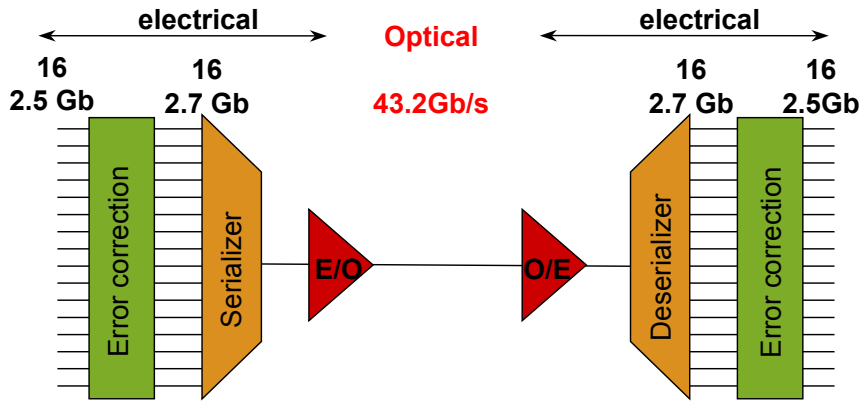
- **Device types**
- **I/O timing definitions**
- **Exploring the unit interval**
- **Optimum sampling points**
- **Differential termination**

Multiplexer / Demultiplexer

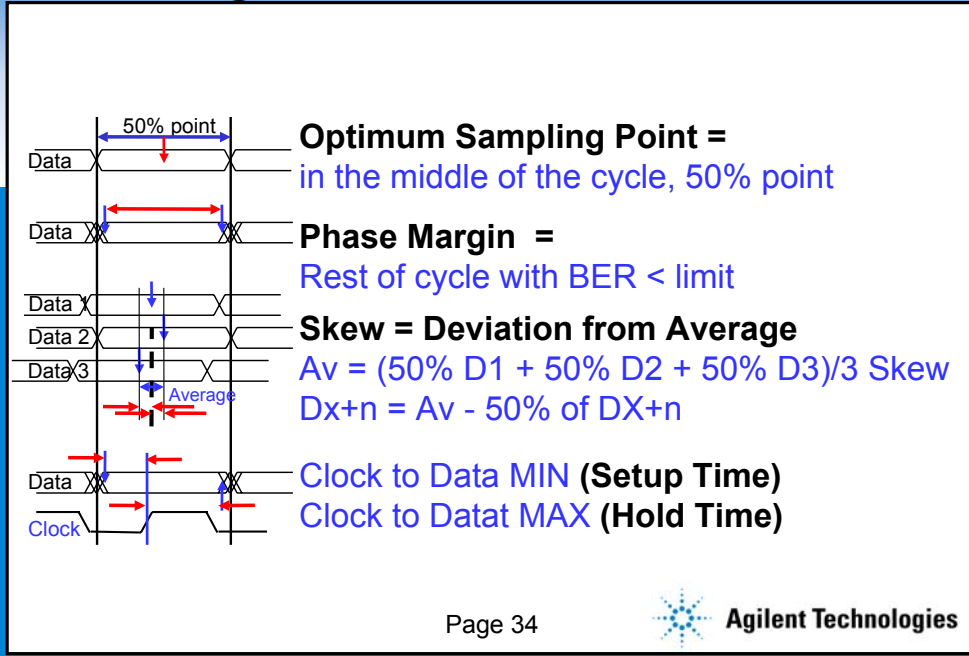
4:1 Multiplexer / 1:4 Demultiplexer



Block Diagram of High-Speed Link



I/O Timing Definitions



Let's begin by discussing specifications for communication devices. In the communication industry, ratios, probabilities, retries, and retransmits are facts of life since the industry realizes that no complex system will work with zero errors unless you are prepared to spend an infinite amount of money.

Therefore, many of the measurements are based on Bit Error Ratios (BER) and BER Threshold limits. Designers of chips in other industries don't deal with such ratios, but use absolute maximum and minimum measured time values instead.

Realizing that, let's define some timing measurements.

- 1) Optimum Sampling Point – is the middle of the data cycle, or 50% point
 - this is the point that provides the most margin from errors due to non-rectangular or jittery waveform shapes
 - most clock recovery circuits adjust the device sampling clocks to this time; however:
 - devices that use an external clock input may not set 50% as “optimum” because the designer is aware of internal device delays
- 2) Phase Margin – is the width of the area of the cycle where the BER is better than the specified Error Threshold limit
 - if the rise and fall times are infinite and there is no jitter, then phase margin equals the period
 - as the clock frequency approaches the device's operating limits, the phase margin decreases because the transition times and jitter become a significant portion of the period
- 3) Skew – is the deviation of the 50% point from the average over all bus lines
- 4) Clock-to-Data min/max -- is the actual time from the clock edge to the V_{out_High} or $V_{out_Low_Low}$ of the channel.
 - Latency/delay from the clock edge until the output reaches the specific high or low voltage levels
 - these are usually equal to the phase margin

Exploring the Unit Interval (Q-factor)

- $Q = (S_1 - S_0)/(\sigma_1 + \sigma_0)$
 - Gaussian noise distribution
 - Amplitude equivalent of SNR
- $BER = \frac{1}{2} \operatorname{erfc}(Q/\sqrt{2})$
 - Decision threshold optimized
 - Relates BER to sensitivity
- Approaches to measuring Q
 - Eye diagram, DCA, and histograms
 - BERT, threshold and sampling point adjustments

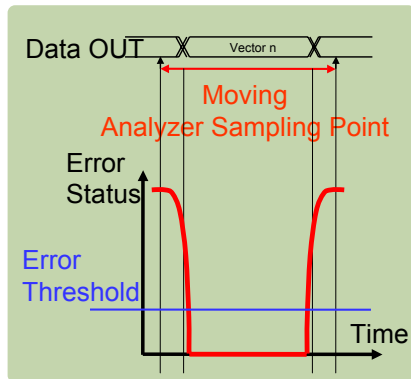
Assuming the amplitude noise associated with the measured signal to be Gaussian in nature, the Q-factor is the delta between mark one and mark zero divided by the sum of the standard deviations of the associated noise contributions. Like other "quality" factor definitions, it is similar to a signal-to-noise ratio, but is measured in terms of signal amplitude rather than power.

One can show that if the decision threshold is optimized to minimize BER, the probability of a bit error becomes proportional to the complementary error function of the Q-factor. Since Q is easily related to received signal and noise power, this expression can be used to calculate system sensitivity.

In order to determine the optimum sampling instant and decision threshold, Q as a function of sampling instant can be measured experimentally using histograms of PRBS eye diagrams on a DCA.

Alternatively, one can derive signal and noise parameters from measured BER as the decision threshold is adjusted into the noise tails and use these directly to calculate the optimum sampling conditions.

Bath Tub Measurement



- **Timing Measurements:**

- **Optimum Sampling Point**
- **Skew**
- **Phase Margin**
- **Setup/Hold Time**
- **Jitter**

The bathtub-shaped plot shown on this slide represents the bit error rate versus time. This plot is used for the evaluation of timing measurements.

Let's talk about this "bathtub" plot in more general terms first. The general shape look similar to an eye opening. The middle of the dip where the errors are low is clearly the opening and the right and left edges where the errors reach their maximum is clearly outside of the eye.

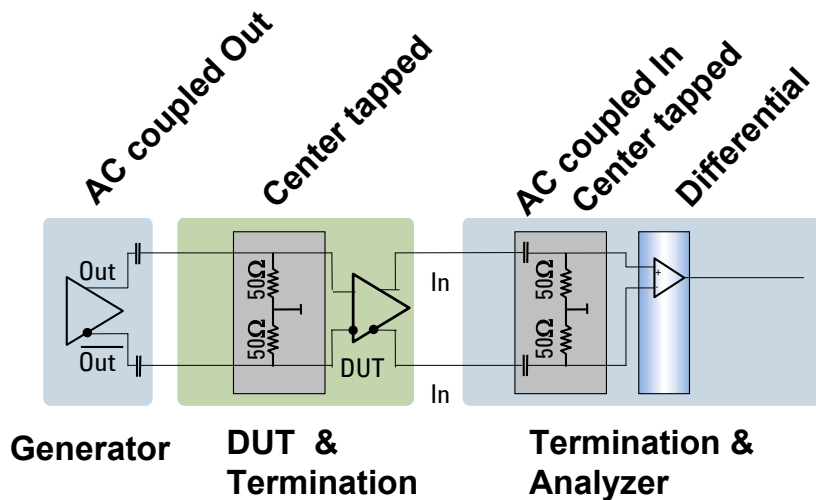
An "ideal eye" would be rectangular, but that is impossible to attain, especially as the operating clock frequency increases. The slope of the edges is proportional to the rise and fall times of the waveform. The "width" of the edges is related to the jitter.

If you allow the measurements to run for a long period of time, you would probably see the edges of the tub getting wider like you would on a scope in infinite persistence. The width of the edges would represent the "jitter."

If the jitter is random the result is represented as RMS, otherwise it would be peak-to-peak.

The Error Threshold is the BER value beyond which the device would be out-of-spec.

Differential Termination



Differential technology is very widely used together with MUX/DEMUX circuitry. Differential means that there is an Output/Input together with complementary Input/Output. The complementary one always deals with the logical opposite of the normal one. So there will never happen same logical level on both, they always will be opposite or complementary (as long as nothing is broken).

The DUT input provides termination for eliminating reflections. This ensures clean signals.

The generator outputs providing the stimulus signals for the DUT are AC coupled. This prevents the application of harmful DC voltages to the DUT. The bandwidth resulting from AC coupling should be low enough so that all low frequency components appearing within the transmitted pattern run through. Practice has proven that a bandwidth of <300kHz is sufficient.

The analyzer connected to the DUT offers differential inputs. This is the right method to detect the proper bit change at the crossing point of the two input signals. It is essential to keep the connection length of both signal lines between DUT and Analyzer input at identical length to maintain the same phase relation at the tester input. The tester input is also terminated together with the AC coupled input.

Q & A

Device Testing

- **Protocol testing**
- **Serial Device**
- **MUX**
- **DMUX**

High Speed Interfaces

Using MUX / DEMUX / Parallel Technology

- **Local Area Networks**
 - Gigabit Ethernet, Fiber Channel, Infiniband, Storage Area Networks
- **Global Networks**
 - Terrestrial, SONET/SDH, Undersea
- **Digital Video**
 - HDTV, Display Links, Flat Panel
- **Components**
 - Backplane serializer / de-serializer, Multiple serial, E/O, O/E

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Local Area Networks

Gigabit Ethernet, Fiber Channel, Infiniband, Storage Area Networks

Serial speed - 2.5 / 3.2Gb/S

MUX 1:10, 1:4

Global Networks

Terrestrial, SONET/SDH, Undersea

Serial speed - 40Gb/s

MUX 1:4, 1:16

Digital Video

HDTV, Display Links, Flat Panel

Serial speed - 1.5Gb/S

MUX 1:7

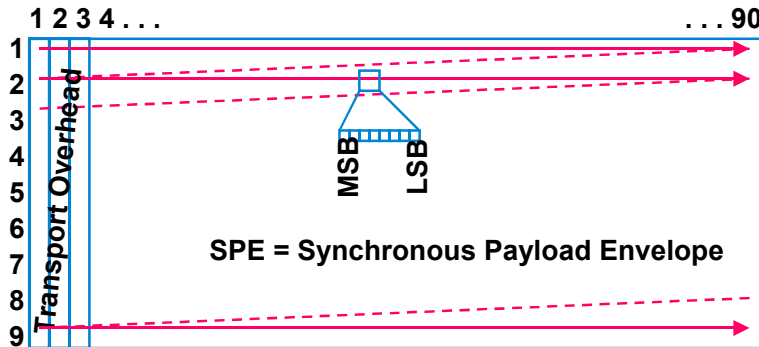
Components

Backplane serializer / de-serializer, Multiple serial, E/O, O/E

Serial speed - various

MUX 1:4, 1:16

SONET Frames



SONET frame = 90 columns x 9 rows = 810 bytes = 6480bits

SONET frame

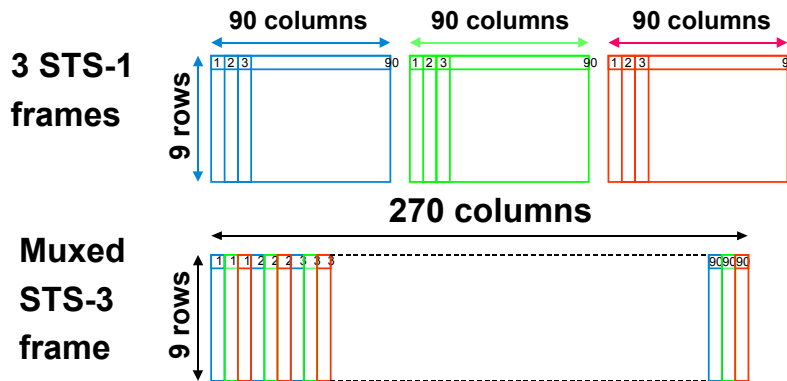
SONET (Synchronous Optical NETwork) is a standardized technology for digital communication. It allows the carrying of multiple signals of different capacities through a synchronous, flexible, optical hierarchy.

This is achieved through byte-wise multiplexing, which supports end-to-end network management. This slide shows the basic or lowest level for (byte-) multiplexing, which consists of 9 rows and 90 columns of bytes, transmitted from left to right and top to bottom, starting with the MSB.

SONET signals are transmitted in a frame structure. In addition to the data payload, the SONET frame includes a header, also known as the transport overhead. This overhead includes data such as the destination address, redundancy check data, etc.

The standard transmission rate (OC-1 (Optical Carrier) or STS-1 (Synchronous Transport Signal)) of this technology is 51.840Mb/s.

SONET Framing (Multiplexing)



OC-/STS-1	SDH-0	51.84
OC-/STS-3	SDH-1	155.52
OC-/STS-12	SDH-4	622.08
OC-/STS-48	SDH-16	2488.32
OC-/STS-192	SDH-64	9953.28
OC-/STS-768	SDH-256	39813.12

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SONET muxing

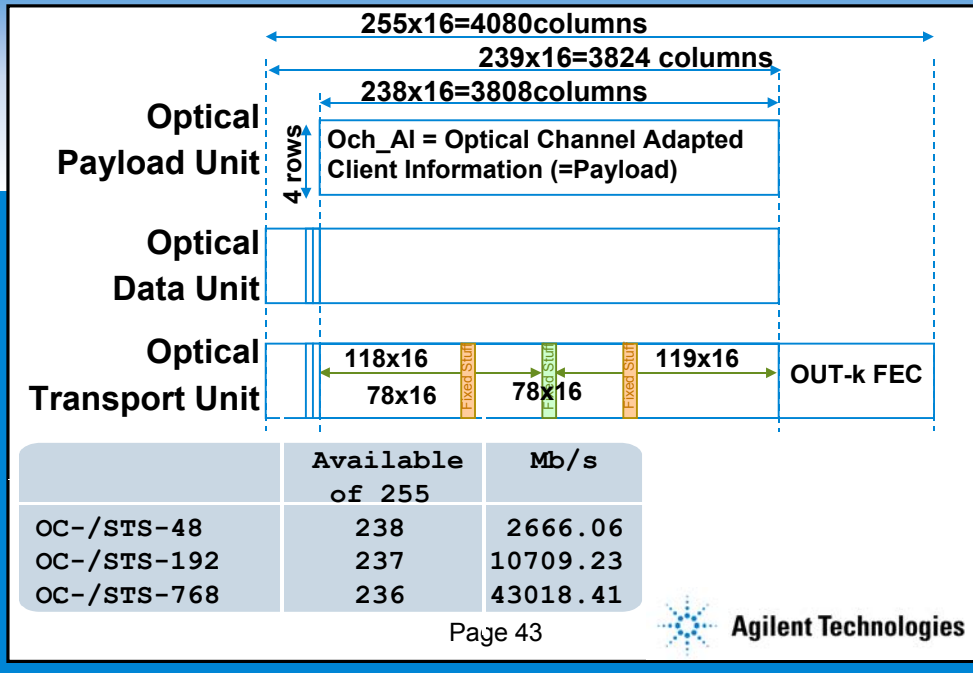
This slide illustrates byte-wise multiplexing from STS-1 to STS-3, raising the data rate from 51.84 MB/s to 155.52 Mb/s. This method starts with the first byte of the first frame, then takes the first byte of the second frame, etc.

The table at the bottom of this slide lists the resulting STS-n/OC-n (SDH) line rates.

SDH

SONET was standardized by ANSI in 1984. In 1989, CCITT issued the SDH (Synchronous Digital Hierarchy) standard, which includes SONET as a subset. As progress was made in terms of line rates, SDH-1 was defined as the equivalent to STS-3.

Forward Error Correction (FEC)



ITU-T G.709: This standard provides requirements for the Optical Transport Hierarchy (OTH) signals at the Network Node Interface in terms of

Definition of an Optical transport module of the order n (OTM-n)

Structures for an OTM

Formats of mapping and multiplexing client signals

Functionality of overhead

We will now discuss how a client payload maps into an optical transport unit and how this mapping (generating the overhead) plus Forward Error Correction change the necessary line rates, particularly because these are different for (the equivalent of) “OC48, OC192” and “OC768”.

Optical Transport Unit-k (OTU-k)

The OTU basically represents that layer before the signal is presented to an “optical modulation unit” for a given wavelength λ , which means data manipulation has been done, including the generation of all necessary overhead, FEC and scrambling.

As for SONET, the basic structure of the OTU is a frame consisting of rows and columns. Unlike SONET, the OTU features only 4 rows and $255 \times 16 = 4080$ columns instead, which are transmitted in the same sense as the SONET frame, i.e. frame from left to right and top to bottom, starting with the MSB.

The OTU contains 1×16 columns (starting with column 1) of ODU/OTU-k overhead, followed by $16 \times 16 = 256$ columns of FEC.

Why Use FEC ?

- Reduce required bandwidth
- Increase throughput
- Reduce transmitter power
- Increase range
- Reduce the required noise figure of the receiver
- Requires BERT with flexible data rate to test various coding schemes

Reduce required bandwidth:

Interchannel interference can be compensated through the use of error correction allowing channels to be closer together.

Increased throughput:

With error correction fewer re-tries are necessary for transmission of the data.

Reduce transmitter power:

The effective sensitivity of system is increased.

Increase Range:

The effective sensitivity of system is increased.

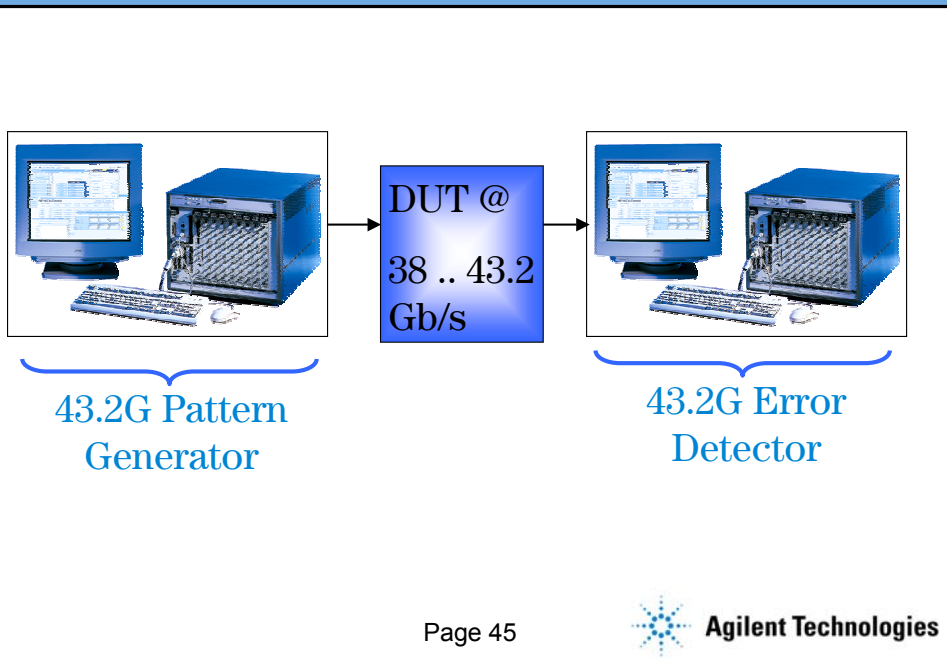
Reduced the required noise figure of the receiver:

With error correction a higher BER can be tolerated and still maintain the same effective BER with the use of error correction.

Flexible BERT design:

Allows for testing of various coding schemes. The R&D engineer can make trade-offs between FEC overhead, bandwidth and BER.

43.2G Serial BERT



Things to keep in mind when testing @ 40Gb/s

Cable length:

Good quality cable can have 7 dB of loss for a 24" length

Differential Drive:

If cables are not matched some means of aligning the DATA and DATA/ is needed

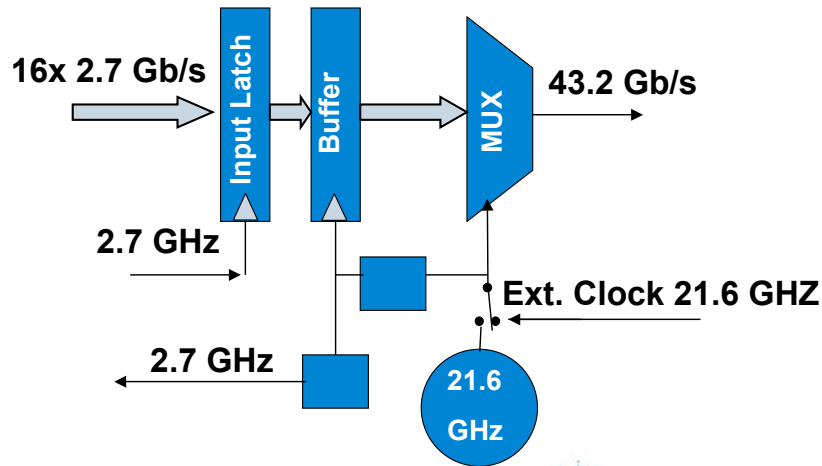
Receiver:

Will the unit operate with single ended signal

Differential Receiver:

If cables are not matched some means of aligning the DATA and DATA/ is needed

Multiplexer Architecture



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The following slides present a proposal for a test system architecture designed to handle data rates of up to 43.2 Gb/s.

Let's begin by looking at the multiplexer architecture inside the DUT.

This slide provides a block diagram of an implementation of a 43Gb/s MUX chip:

This setup uses an internal oscillator. Alternatively, an external clock could be applied.

The clock is double pumped, running at 20GHz.

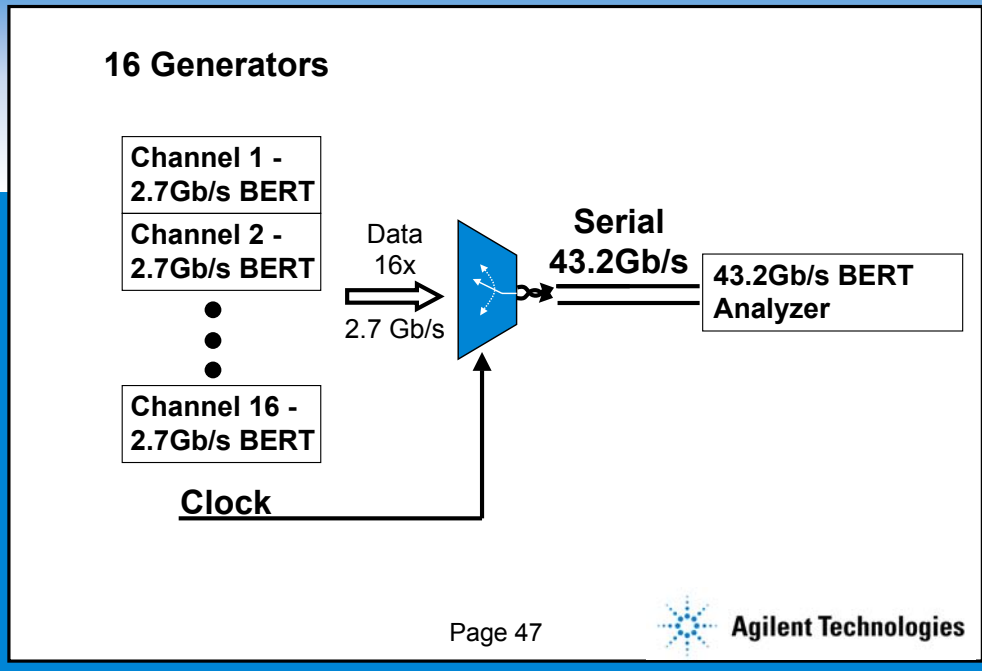
3. This clock drives the final MUX stage as well as (divided by 8) the intermediate buffer stage.

4. This divided clock is also provided to the low speed data input port through a phase shifter.

This phase shifter can be used to compensate the delay through the loop into the ASIC providing the data for proper setup and hold times.

5. The input buffer latches the data from the framer ASIC.

MUX Test Setup



Now let's take a look at the setup for testing a 43Gb/s MUX chip.

We need stimulus signals (on the left side) as well as analyzing capabilities. Let's look at the stimulus first:

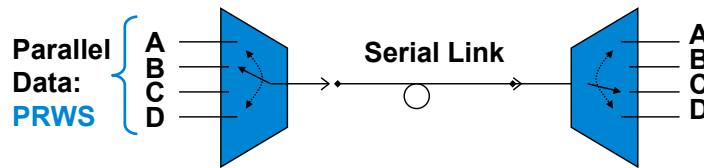
1. 16 Generators provide the data at 2.7Gb/s which the MUX chip puts together.
2. A synthesizer provides the clock for running the data generation and the DUT.

The analysis needs to be done on the 43Gb/s signal.

1. The DUT (shown in blue) is connected to a BERT analyzer which first performs CDR (Clock-Data-Recovery) and then de-muxes the high speed data into 16 x 2.7Gb/s data.
2. The data processing and error checking is performed.

PRWS Data

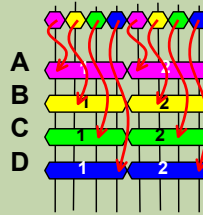
(Pseudo Random Word Sequence)



PRWS is defined by:

- Polynomial $2^n - 1$
- Algorithm
- Parallel bus width

PRBS:



PRWS stands for: Pseudo Random Word Sequence.

This sounds similar to PRBS, except for “word.” Sounds like it might have something to do with parallel – and it does!

PRWS is the magic algorithmic parallel pattern that results in the appropriate PRBS after a MUX operates on it. Additionally, you could expect that a DEMUX would convert a PRBS into the appropriate PRWS.

As expected, parallel BERTs can create parallel “words” with two parameters – number of bits in the word and the PRBS polynomial we want to see on the output.

Let's see how it works!

If you look at our 4-to-1 MUX/DEMUX link, you would expect that the serial line should have the PRBS we want to test our devices with since this is the serial line that connects into the actual network.

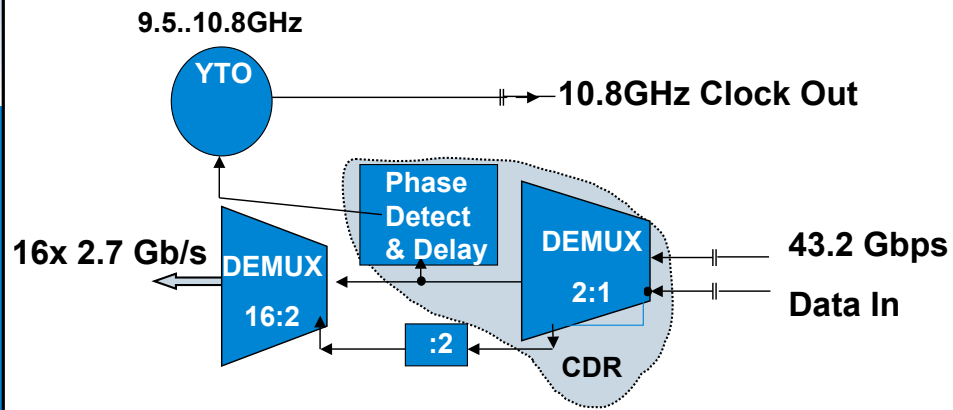
Remember that the 4:1 MUX ratio means that data coming out of the MUX is clocked at a rate 4 times faster than the input data is being latched. This is represented by bit colors and numbered words on the left.

The slide shows that the PRBS is the result of the multiplexing action – latch at rate f , then shift out a rate $4f$.

The PRWS is like the PRBS, except that PRWS is sliced into segments – words – whose length expresses the MUX/DEMUX ratio. To keep things simple, the parallel BERT generates the proper sequence of words that will create the proper PRBS.

On the other hand, if another digital test system cannot create this special word sequence, then that system cannot stimulate or analyze these devices realistically.

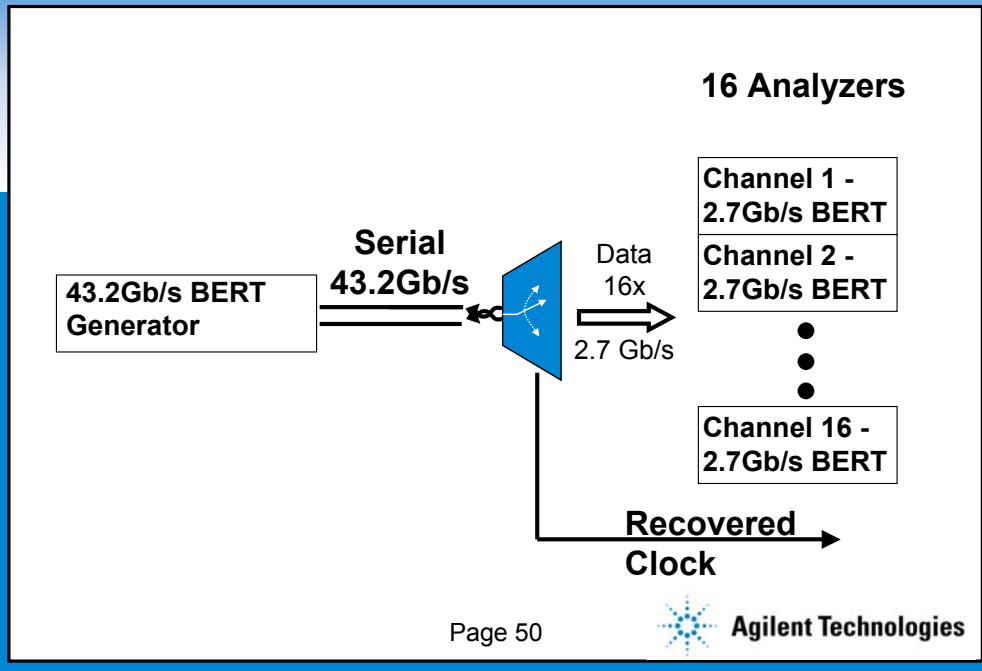
43.2G DEMUX Module Architecture



This block diagram shows a DEMUX module architecture.

A 1:2 DEMUX makes up the first stage of this module. The CDR is located downstream of this DEMUX, so the recovered clock runs at 20GHz. The divided recovered clock drives a second 2:16 DEMUX stage.

DEMUX Test Setup



This slide shows the setup for testing a DEMUX.

Again, the stimulus side is shown on the left and the analysis side is shown on the right.

Stimulus side

1. One 43Gb/s data stream is supplied to the DUT
2. The MUX module receives a clock signal from a synthesizer for best clock performance. The clock signal is divided to provide a reference for the 16 data generators.
3. The DEMUX receives the data stream. It does not need any clock as it has its own internal CDR.

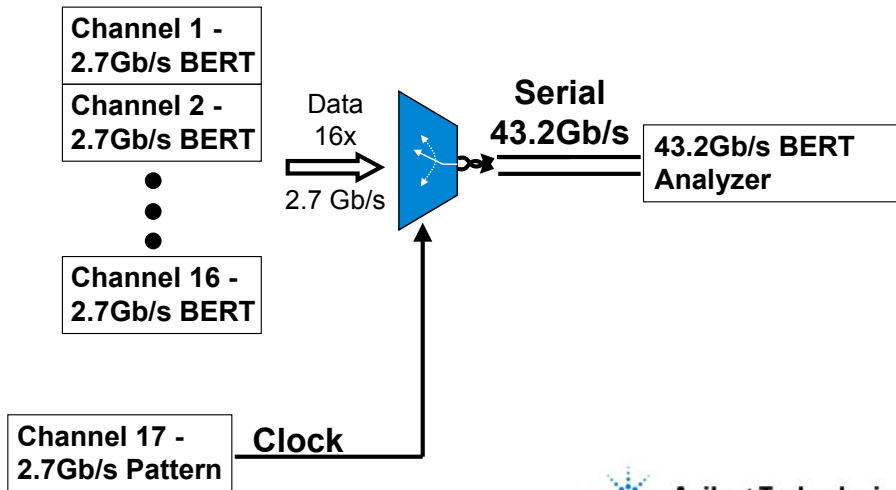
The DEMUX chip puts out 16 data streams at 2.7Gb/s together with a recovered clock.

Analysis side

The analyzer consists of 17 channels, 16 of which are used for BER testing, while the 17th analyzer measures the clock timing so that the output timing measurement can be performed.

SONET-FRAMER-INTERFACE SFI 5

16 Generators

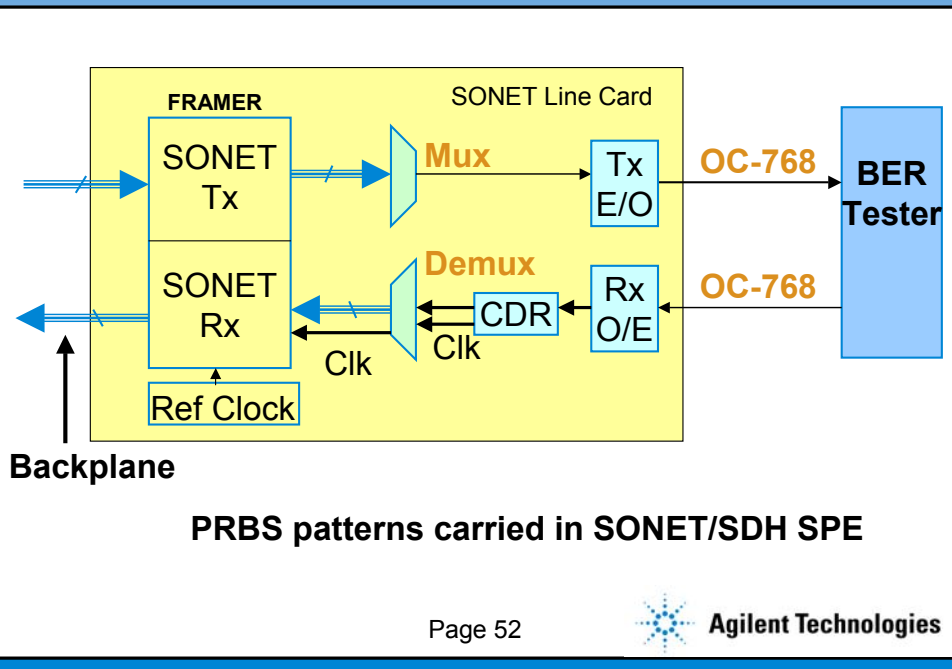


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SFI-5 Description

SONET Line Card Test Application



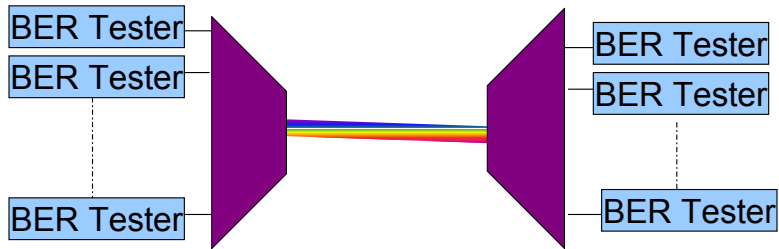
For a SONET Line card the BERT must be able provide optical signals at the 40GB/s rate as well as receive optical signals at that rate.

The optical signal generation is usually done with an external modulator.

Depending on the line card the coding scheme can be non-return-to-zero (NRZ) or return-to-zero (RZ). Typically NRZ is used in short haul networks and RZ used in long haul networks.

A flexible BERT should be able to provide both types of coding schemes to allow for testing of various types of line cards.

DWDM Test System



Alternative is to use bank of DFBs and modulate even channels with DATA and odd channels with DATA

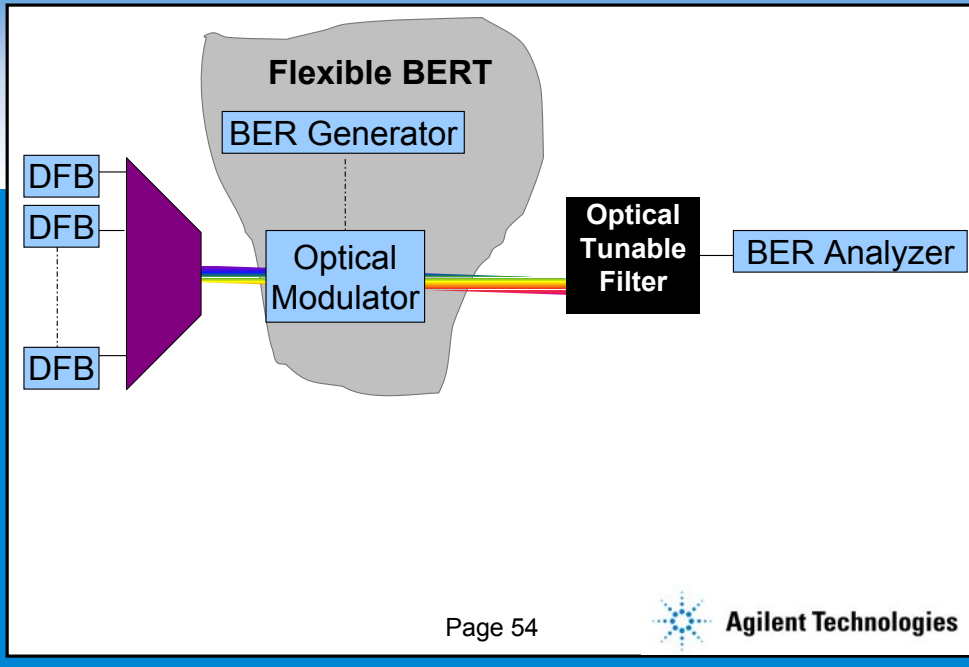
The illustrated solution would be great for manufactures of BERTs. Think of the number of units that would have to be bought and the expense.

An alternative is to use a single BER Generator and two modulators. Alternate optical channels would be modulated with DATA and DATA/.

On the receive side a tunable optical fileter would be used to select the channel to be measured and sent to a single BER analyzer.

This setup is illustrated in the following slide.

DWDM Test System (alternative)



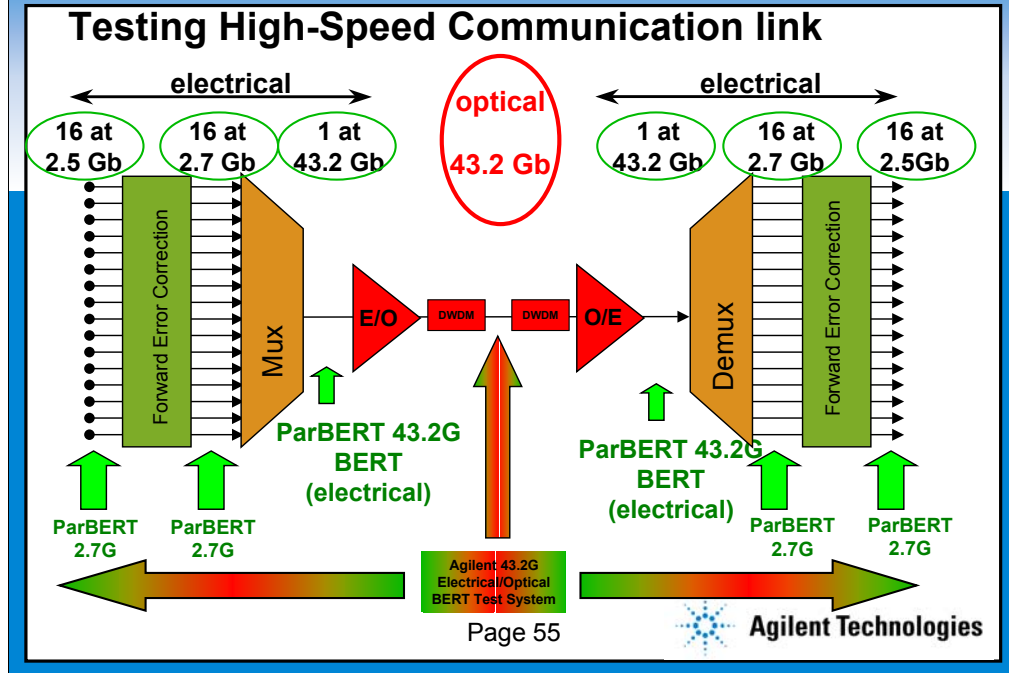
The illustrated solution would be great for manufactures of BERTs. Think of the number of units that would have to be bought and the expense.

An alternative is to use a single BER Generator and two modulators. Alternate optical channels would be modulated with DATA and DATA/.

On the receive side a tunable optical fileter would be used to select the channel to be measured and sent to a single BER analyzer.

This setup is illustrated in the following slide.

Total Integrated 43G Solution



Highly flexible BERT design allows for testing MUX, DMUX, in line components in any combination of of Electrical or Optical.

The required data stream is tapped off and measured.

Conclusion

- **The challenges involved in testing 40Gb/s devices can be met with existing technology**
- **Improvement in technology will allow quicker and more accurate characterization of devices**
- **Flexible BERTs allow for ease in testing of various device configuration**
- **Memory based BERTs allow for simulation of protocol for testing of many devices**

Q & A